

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Vincent Dupaquis et al.

PATENT APPLICATION

Serial No.: 10/615,476

Group Art Unit: 2124

Filed: July 7, 2003

Examiner:

For: COMBINED POLYNOMIAL AND NATURAL  
MULTIPLIER ARCHITECTURE

Supplemental Information Disclosure Statement

Hon. Commissioner for Patents  
Alexandria, VA 22313

Sir:

The following information is submitted in compliance with Applicants' duty of disclosure under 37 CFR § 1.56. Copies of three of the four references are enclosed. We are unable to obtain a copy of the last reference listed (marked by an asterisk).

Other References

C.S. Wallace, "A Suggestion for a Fast Multiplier", IEEE Transaction on Electronic Computers, February, 1964, pages 14-17.

M.J. Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley, 1987, 5 pages.

Website printout: vlsi.wpi.edu/webcourse, D. Mlynek and Y. Leblebici, Design of VLSI Systems, "Arithmetic For Digital Systems", Chapter 6, 1998, 39 pages.

\*Paper by Dadda, from a paper presented at the Colloque sur l'Algebre de Boole, Grenoble France, Jan. 1965.)

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Asst. Commissioner for Patents, Alexandria, VA 22313

Signed: Sally Azevedo  
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Date: October 16, 2003

Respectfully submitted,

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Sheet 1 of 1

FORM PTO-1449			Atty. Docket No. ATM-213		Serial No. 10/615,476	
LIST OF PRIOR ART CITED BY APPLICANT			Applicant: Vincent Dupauquis et al.			
			Filing Date: July 7, 2003		Group: 2124	
U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Grant Date	Name	Class	Sub Class	Filing Date
	AA					
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
FOREIGN PATENT DOCUMENTS						
Examiner Initial*	Document Number	Grant Date	Country	Class	Sub Class	Translation Yes No
	AH					
	AI					
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
	AJ	C.S. Wallace, "A Suggestion for a Fast Multiplier", IEEE Transaction on Electronic Computers, February, 1964, pages 14-17.				
	AK	M.J. Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley, 1987, 5 pages.				
	AL	Website printout: vlsi.wpi.edu/webcourse, D. Mlynek and Y. Leblebici, Design of VLSI Systems, "Arithmetic For Digital Systems", Chapter 6, 1998, 39 pages.				
	AM	Paper by Dadda, (from a paper presented at the Colloque sur l'Algebre de Boole, Grenoble France, Jan. 1965.) (no copy enclosed)				
EXAMINER:				DATE CONSIDERED:		
*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						